Q.P. Code: 16CS506 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations November-2020

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 **a** Convert the following numbers (L5) (3M) **6M**

i) $(AB)_{16} = (\ )_2$

ii) $(1234)_8 = (\ )_{16}$

iii) $(101110.01)_2 = (\ )_8$

b Convert the given to binary and then to gray code **6M**

$(AB33)_{16}$

OR

2 **a** Simplify the Boolean expressions to minimum number of literals **6M**

i) X' + XY + X Z' + XYZ'

ii) (X+Y) (X+Y')

b Obtain the Complement of Boolean Expression **6M**

i) A+B+A'B'C

ii) ii)AB + A (B +C) + B'(B+D)

UNIT-II

3 Obtain the minimal product of sums and design using NAND gates **12M**

$F(A,B,C,D) = = \Sigma m(0,2,3,6,7) + d(8,10,11,15)$

OR

4 Simplify the Boolean expression using K-MAP (L5) (10M) **12M**

$F(A,B,C,D) = \pi M\ (3,5,6,7,11,13,14,15)\ .d(9,10,12)$

UNIT-III

5 Explain Carry Lookahead Generator? **12M**

OR

6 **a** Design a 4 bit binary parallel subtractorand the explain operation in detail? **6M**

b Design the combinational circuit of Binary to Excess-3 code convertor? **6M**

UNIT-IV

7 **a** Explain the Logic diagram of SR flip-flop? **6M**

b Design and draw the 3 bit up-down synchronous counter? **6M**

OR

8 **a** Write the differences between latches and flip flops? **6M**

b Write the differences between synchronous and asynchronous counters? **6M**

UNIT-V

9 Implement the following function using PLA **12M**

$A(x,y,z)=\Sigma m(1,2,4,6)$,$B(x,y,z)=\Sigma m(0,1,6,7)$ and $C(x,y,z)=\Sigma m(2,6)$

OR

10 Design PAL for a combinational circuit that squares a 3 bit number? **12M**

*** END ***